# 5-GHz BAND 30 WATT POWER GaAs FETS

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## Abstract

C-band high-power and high-efficiency GaAs FETs have been developed. The active region of FET chip has been highly integrated by forming long gate fingers. Four chips are power-combined efficiently by using internal matching circuits.

The FETs deliver an output power at 1dB gain-compression point of 30W with 6.8 dB gain and 28 % power-added efficiency, and a suturated output power of 33 W at 5.5 GHz. These output powers are the highest values reported so far on power GaAs FET. Moreover they exhibit an excellent linearity with a third-order intermodulation distortion intercept point of +55 dBm.

## Introduction

High-power and high-efficiecy GaAs FETs are essential for amplifier applications in radar systems and digital communication systems. C-Band power GaAs FETs with 20 W output power [1] have already been commercially available. In order to achieve better device perfomance, it is indispensable that the device is integrated as highly as possible and the multichip output powers are efficiently combined.

The purpose of this paper is to report on a 5-GHz-band multichip-operated internally-matched power GaAs FET with more than 30 W output power. Four chips are power-combined to attain such a high output level, with each chip size equal to the chip size of the four-chip 20 W device reported earlier [1].

## Device Fabrication

An n-type channel layer is formed by selective implantation of Si ions, first at 80 keV with a dose of $1.3 \times 10^{12}$ cm$^{-2}$, and secondly at 250 keV with a dose of $3.7 \times 10^{12}$ cm$^{-2}$. Then, ion implantations with a dose of $2.0 \times 10^{13}$ cm$^{-2}$ are performed succesively at 50 keV, 120 keV and 250 keV to form $n^+$ layers for source and drain. The implanted wafers are capless-annealed at 850 ℃ for 15 minutes in pure argon ambient containing a small amount of arsine ($AsH_3$). The peak carrier concentration of channel layer is about $1.3 \times 10^{17}$ cm$^{-3}$ measured by C-V method.

The source and drain ohmic contacts are formed by alloying Pt/AuGe. The aluminum gate is delineated by deep-UV lithography and passivated with $SiN/SiO_2$ film.

## Device structure

The FET chip has been designed to highly integrate the active region. In this respect, longer gate finger width is desirable. Although the channel temperature rise is insensitive to gate-finger width W when W is much longer than the substrate thickness, microwave signal attenuation along the gate finger increases with W. Taking these into consideration, W has been chosen to be 280 $\mu$ m for 5-GHz operation.

Fig.1 shows the top view of the FET chip. The gate length and the total gate width are 1.3 $\mu$ m and 25 mm, respectively. The substrate thickness is about 80 $\mu$ m. The chip size is 3.0 mm × 0.8 mm, which is the same size as that of the FET chip with 14.4 mm gate width reported previously [1].

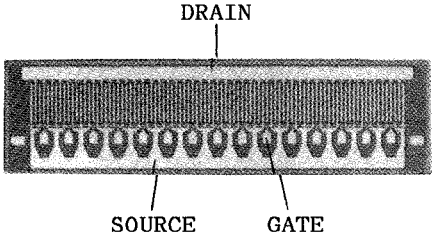


Fig.1 Top view of FET chip
(total gate width=25mm,
chip size=3.0mm × 0.8mm)



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One-chip and four-chip devices are internally matched at both input and output ports using lumped and distributed elements. Fig.2 shows the internal view of the 4-chip device which has a total gate width of 100 mm.

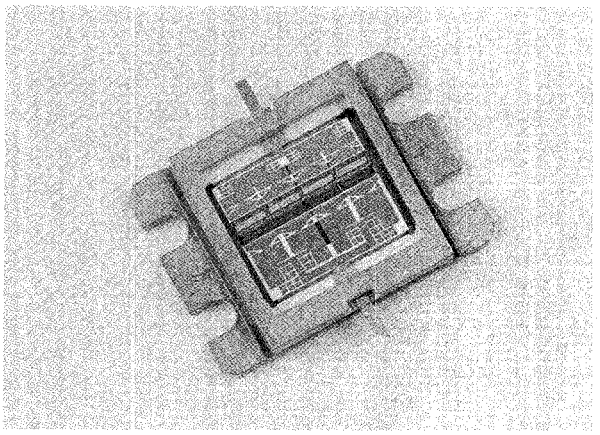

Fig.2 Internal view of 4-chip device (total gate width=100mm)

## FET performance

Typical saturated drain current, transconductance, and pinch-off voltage are 20A, 6.1 S, and 3.6 V, respectively, for the 4-chip internally matched FET. The gate to drain breakdown voltage is typically -10V at a leak current level of 400 $\mu$A. A typical thermal resistance has been found to be about 1.0 ℃/W from IR scanning microscope measurement. The channel temperature rise, $\Delta$ Tch, is estimated to be about 60 ℃ when the device delivers 30 W output power.

The rf performances of the 1-chip and 4-chip devices at 5.5 GHz under a drain-source voltage of 10 V are shown in Fig.3. The 1-chip device delivers an output power at 1dB gain-compression point ($P_{1dB}$) of 10.5 W with 7.8 dB gain and 36 % power-added efficiency. A $P_{1dB}$ of 30 W has been obtained with 6.8 dB gain and 28 % power-added efficiency from the 4-chip device. The power-combining efficiency of the 4-chip device is about 70 %. A typical output power v.s. frequency characteristic of the 4-chip device is shown in Fig.4, where the input power is 38 dBm.

More than 30 W of output power is obtained over 5.3 to 5.5 GHz. Fig.5 shows the third order intermodulation distortion characteristic of the 4-chip device at 5.5 GHz under a two-tone test with a frequency separation of 5 MHz. An intercept point of +55 dBm has been obtained. Such an excellent linearity is most desirable to digital communication system applictions.

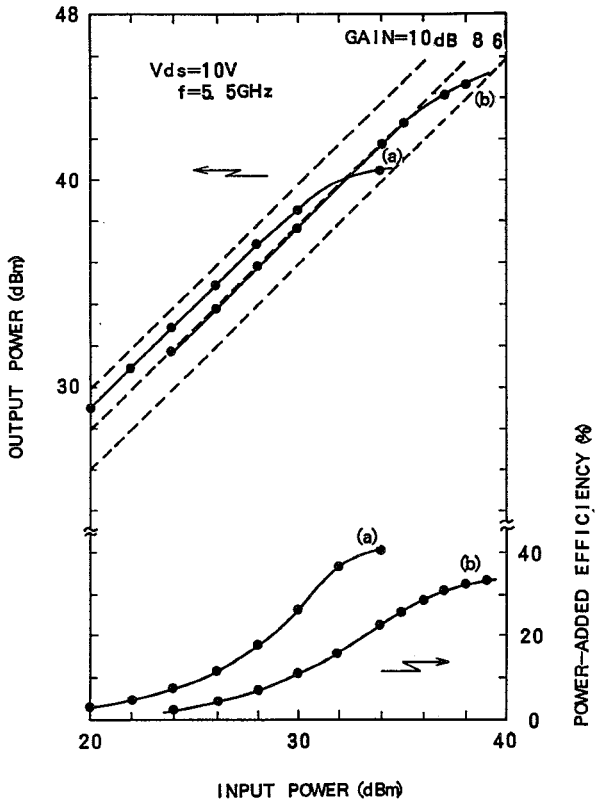


Fig 3 Output power and power-added efficiency versus input power at 5 5GHz for (a) 1-chip and (b) 4-chip devices

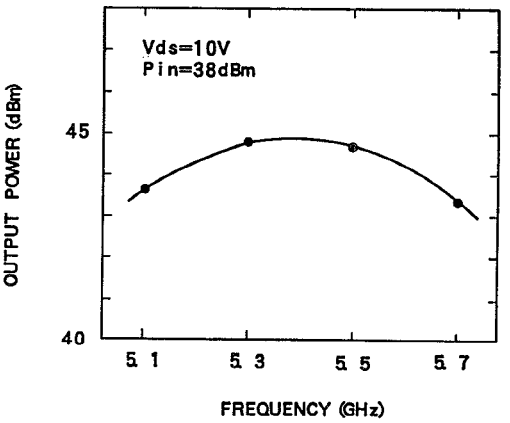


Fig 4 Output power versus frequency of 4-chip device

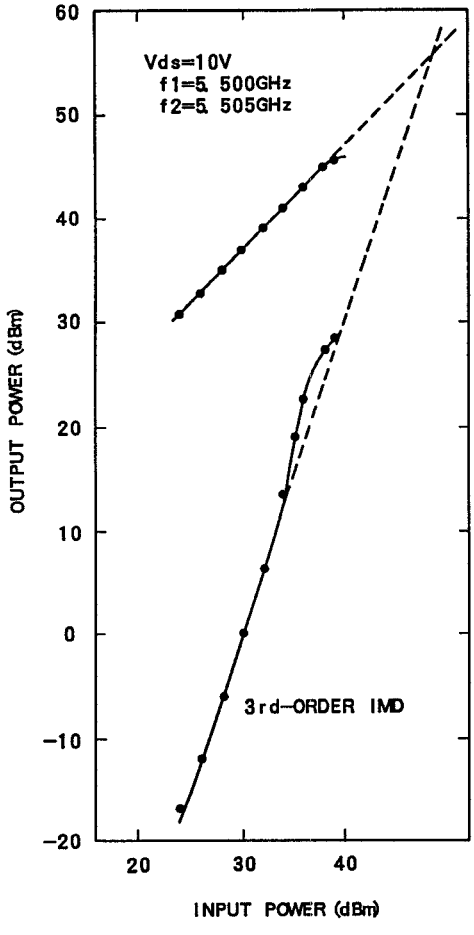


Fig. 5 Third order intermodulation distortion characteristic of 4-chip device

## Conclusions

C-band high-power multi-chip internally-matched GaAs FETs have been developed. At 5.5 GHz, an output power at 1dB gain-compression point of 30 W has been obtained with 6.8 dB gain and 28 % power-added efficiency from the 4-chip device with a total gate width of 100 mm. This device gives more than 30 W of output power over 5.3 to 5.5 GHz. Moreover, it shows an excellent linearity with the third-order intermodulation intercept point of +55 dBm at 5.5 GHz.

The attained results contribute to improve the performance of various microwave systems.

## Reference

[1] S.Yanagawa,et al.,"High-power and high-efficiency ion-implanted power GaAs FETs for C and X band",in 1985 IEEE MTT-S Int. Symp. Dig., pp. 332-335.